What Is Claimed Is:

1. A configurable unit that can be reconfigured at run time controlled by a primary logic unit (PLU) for processing arithmetic and logic operations (PAE) for use in central processing units (CPUs), multi-processor systems, data flow processors (DFPs), digital signal processors (DSPs), systolic processors and field programmable gate arrays (FPGAs), characterized in that

a. a programmable arithmetic and logic unit (EALU) is provided for performing the basic mathematical and logic functions,

b. the function and interconnection of the central processor are programmed in registers and various data can be processed without reprogramming the PAE,

c. there is a state machine (SM UNIT) for controlling the arithmetic and logic unit (EALU),

d. registers are provided for each operand (O-REG) and the result (R-REG), some of the registers being designed as shift registers,

e. there is feedback of the data of the result register to an input of the EALU over a multiplexer (R2O-MUX),

f. a bus unit (BM UNIT) permits pick-up of data from a bus system and feeding the result to a bus system, the bus unit being capable of sending data to multiple receivers and the synchronization of multiple receivers taking place automatically,

g. the bus access from the data processing in the EALU is decoupled via the registers and thus each PAE can be regarded as an independent unit, in particular the configuration and reconfiguration of a PAE have no interfering effect on the data transmitters and receivers or on the independent PAEs,

h. the sequence of bus transfers is controlled automatically using a state machine (sync UNIT), for which purpose handshake lines oRDY, oACK, rRDY and rACK are available, and

i. feedback is sent to the PLU for detection of the processing status and reconfigurability of the PAE (state-back UNIT).

2. The unit according to Claim 1, characterized in that the data processing of a PAE can be stopped (STOP entry in F-PLUREG) and the PAE then indicates its readiness for reconfiguration (ReConfig) after completing the data processing currently underway.

3. The unit according to Claim 1, characterized in that there are power-saving modes

a) in which the PAE always operates only when operands from the data transmitter are available at the input and the result has already been accepted by the receiver, and the PAE otherwise remains inactive without a clock pulse,

b) in which partial areas of the PAE which are irrelevant for the execution of the data processing currently underway are separated from the clock pulse supply and/or the power supply, in which the PAE is separated from the power supply.